BEEcube

# BEEcube Academic Program

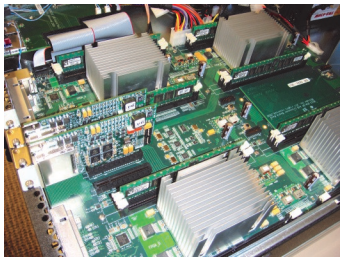
BEE3 systems are currently being utilized in numerous world leading universities such as:

- Stanford University, USA
- Massachusetts Institute of Technology, USA
- University of California Berkeley, USA
- Carnegie Mellon University, USA
- Tokyo University, Japan
- Cambridge University, United Kingdom
- Tsinghua University, China
- University of California Los Angeles, USA
- Peking University, China
- North Carolina State University, USA
- University of Michigan, USA
- University of California, San Diego, USA
- Pennsylvania State USA
- University of Alabama in Huntsville, USA
- Barcelona Super Computing Center, Spain
- University of Cyprus, Cyprus
- Leiden University, Netherlands
- Technische Universitat Darmstadt, Germany
- Anadolu University ,Turkey


Evolved from the original Berkeley Emulation Engine (BEE), BEE3 is the third generation commercial FPGA based computer system. Jointly developed by Microsoft Research, UC Berkeley, and BEEcube Inc., the BEE3 system design draws from lessons learned in previous generations and from over 40 years of design experience of the legendary computer architect and Turing Award winner Chuck Thacker, BEE3's chief designer. Today there are over 150 BEE systems used worldwide. In addition, over 50 academic and research papers have been published for a wide range of applications including: multi-core computer architecture, wireless communications, 100Gbps+ Networking Solutions, HD video processing, signal intelligence, radar/sonar array, bioinformatics, data mining, medical imaging, and more.

## BEEcube Academic Discounts & Donations

As a Third Party Alliance member of the Xilinx University Program (XUP), BEEcube offers special discounts and donations to academic institutions worldwide. This program strives to make the latest FPGA based computer systems available to higher education and research communities on a whole range of application domains.



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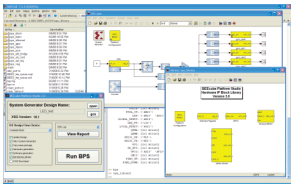
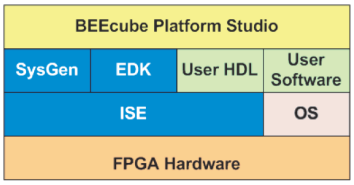
# BEEcube Platform Studio for Academic Users

BEEcube Platform Studio (BPS) is a system-level, hardware/software co-development environment on top of the MathWorks™ Simulink® framework. BPS provides automatic generation of all platform specific hardware interfaces and corresponding software drivers. Months of engineering tasks to convert complex DSP algorithms to implementation can be achieved through BPS in a matter of days, all without requiring user knowledge of the low level FPGA implementation details, such as high speed I/O interfaces, timing closure, HW/SW interfaces, and IP integration issues.






A special academic edition of BPS is currently offered to universities worldwide free of licensing fees. The BPS-AE supports the latest Xilinx XUP-V5 hardware platform.

## Selected Publications Referencing BEEcube Systems


- **Base-Calling in DNA Pyrosequencing with Reconfigurable Bayesian Network**, by Mingjie Lin and Yaling Ma of Stanford University, *RECONFIG '09: Proceedings of the 2009 international conference on reconfigurable computing and FPGAs*, December 2009.
- **Implementing a High-Performance Multithreaded Microprocessor: A Case Study in High-Level Design and Validation**, by Eric S. Chung and James C. Hoe of Carnegie Mellon University, *MEMOCODE '09: Proceedings of the 7th IEEE/ ACM international conference on formal methods and models for codesign*, July 2009.
- **Internet-in-a-Box: Emulating Datacenter Network Architectures using FPGAs**, by Jonathan D. Ellithorpe, Zhangxi Tan, and Randy Katz of University of California at Berkley, *DAC '09: Proceedings of the 46th annual Design Automation Conference*, July 2009.
- **ProtoFlex: Towards Scalable, Full-System Multiprocessor Simulations Using FPGAs,** by Eric S. Chung, Michael K. Papamichael, Eriko Nurvitadhi, James C. Hoe, Ken Mai and Babak Falsafi of Carnegie Mellon University, *Transactions on Reconfigurable Technology and Systems (TRETS),* Volume 2 Issue 2, June 2009.
- **Performance and Power of Cache-Based Reconfigurable Computing**, Andrew Putnam, Susan Eggers, Dave Bennett, Eric Dellinger, Jeff Mason, Henry Styles, Prasanna Sundararajan and Ralph Wittig of University of Washington in collaboration with Xilinx, *ISCA '09: Proceedings of the 36th annual international symposium on computer architecture*, June 2009.
- **Accelerating Monte Carlo Based SSTA using FPGA**, by Jason Cong, Karthik Gururaj, Wei Jiang, Bin Liu, Kirill Minkovich, Bo Yuan and Yi Zhou of University of California at Los Angeles
- **A Message-Passing Hardware/Software Co-Simulation Environment for Reconfigurable Computing Systems**, by Manuel Saldana, Emanuel Ramalho and Paul Chow of University of Toronto, *International Journal of Reconfigurable Computing*, Volume 2009, January 2009.
- **A Multi-FPGA Application-Specific Architecture for Accelerating a Floating Point Fourier Integral Operator**, by Jason Lee, Lesley Shannon, Matthew J. Yedlin, and Gary F. Margrave of Simon Fraser University with University of British Columbia and University of Calgary, *ASAP '08: Proceedings of the 2008 International Conference of Application Specific Systems, Architectures and Processors*, July 2008.
- **Reconfigurable Computing for Learning Bayesian Networks**, by Narges Bani asadi, Teresa H. Meng, and Wing H. Wong of Stanford University, *FPGA '08: Proceedings of the 16th international ACM/AIGDA symposium on FPGAs,* February 2008.
- **RAMP: Research Accelerator for Multiple Processors**, by John Wawrzynek, David Patterson, Mark Oskin, Shih-Lien Lu, Christoforos Kozyrakis, James C. Hoe, Derek Chiou and Krste Asanovic of University of California at Berkeley with University of Washington, Stanford University, Intel, Carnegie Mellon University, University of Texas, and the Massachusetts Institute of Technology, *IEE Micro*, Volume 27 Issue 2, December


For an expanded list of publications, please refer to the BEEcube in Academic Research Brochure. E-mail sales@beecube.com for more information.