



### Multi-core SoC Design

Real-time prototyping of large scale next generation multi-core System-on-Chip designs with ease

### High Performance DSP

Create complex digital signal processing applications with tera operations per second throughput

### HD Video Processing

High definition video processing with multiple real-time 1080p video data streams

### Cognitive Radio and Wireless Communications

Ultra-wide-band wireless communications implementation with multi-GHz A/D and D/A interfaces

### Bioinformatics

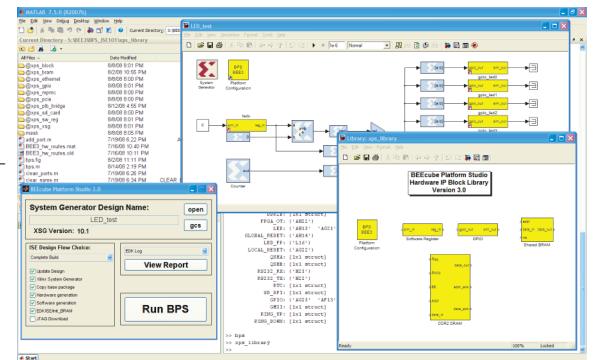
Make sense out of enormous data sets created by bioinformatics observations

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# BEEcube Platform Studio

BEEcube Platform Studio (BPS) is a system-level, hardware/software co-development environment on top of the MathWorks™ Simulink® framework. BPS provides automatic generation of all platform specific hardware interfaces and corresponding software drivers. Months of engineering tasks to convert complex DSP algorithms to implementation can be achieved through BPS in a matter of days, all without requiring user knowledge of the low level FPGA implementation details, such as high speed I/O interfaces, timing closure, HW/SW interfaces, and IP integration issues.



### What is a Platform?

BEEcube Platform Studio			
SysGen	EDK	User HDL	User Software
ISE			OS
FPGA Hardware			

Each BPS platform is a collection of hardware devices and associated software available on the physical module. The BPS platform has been purposefully built to abstract hardware specific details away from the end user. The smallest unit of the BPS platform is a single FPGA.

A typical design in the BPS design environment starts with the core algorithm design in Simulink with Xilinx System Generator for DSP. From the end-user perspective, Simulink designs only exist in a protected sandbox with the synchronous data flow execution model; all connections outside the core algorithm are virtually mapped through BPS interface block sets.

A processor core, either in the form of a hard core (PowerPC 405) or soft core (MicroBlaze™ processor), is implicitly included in all BPS designs. The processor core can communicate with the user XSG design through software registers, FIFO, or shared memory. Users can specify the desired communication method by selecting the corresponding BPS blocks in Simulink. All external network, I/O, and memory devices are abstracted into Simulink data sources or sinks, with a simple FIFO abstraction.



### Turnkey Solution

Everything a designer needs to successfully create a compelling application, from hardware to software, interface IPs to operating systems

### Technical Support

Experienced technical support staff is available for immediate response within 1 business day via email or telephone

### Design Services

Accelerate your next project development with our dedicated services from application domain experts

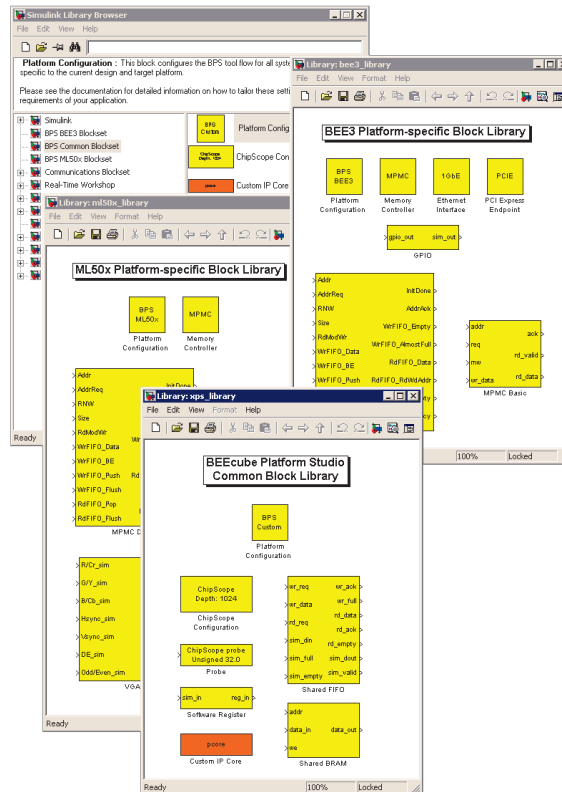
### Endless Solutions

Go beyond the basics to next level of integration with our expanding collection of expansion modules, specially designed to meet your application needs

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## BPS Libraries



### HW/SW Interfaces

- Shared BRAM
- Software Register
- Shared FIFO

### External Memory

- ZBT SRAM
- DDR2 ECC DRAM
- Multi-port memory controller

### High Speed Networks

- Tri-mode Gigabit Ethernet & TCP/IP Stack
- Aurora Interfaces
- 10G Ethernet & XAUI

### System I/Os

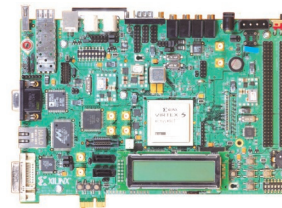
- GPIO up to DDR800 data rates
- Multi-GHz ADC & DAC
- HD Video VGA/DVI

### Debug Interface

- ChipScope Integration
- HW Co-simulation
- XMD Software Debugger

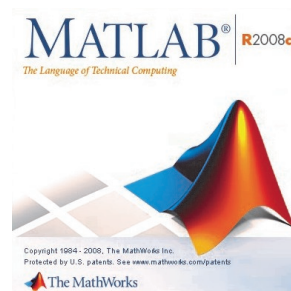
## FPGA Platforms Supported

- BEEcube BEE3
- Xilinx ML505/506/507
- Xilinx XUP-V5
- MORPH VITA-46
- MORPH VH/VL/PH/PMC



## Third Party Software Requirements

- MathWorks MATLAB/Simulink 2007b or later
- Xilinx ISE 10.1i SP3 or later
- Xilinx EDK 10.1i SP3 or later
- Xilinx System Generator 10.1i SP3 or later
- Xilinx ChipScope 10.1i SP3 or later (optional)
- Mentor Graphics ModelSim 6.3a or later (optional)



Support both Windows and Linux OS

