

MORPH V2P Product Line

Reconfigurable Signal Processors



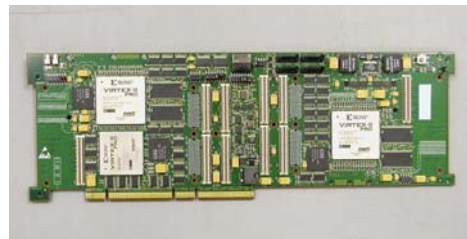
MORPH VH



MORPH VL



MORPH PMC



MORPH PH

Product Description

The MORPH V2P product line is based on reconfigurable board level logic. Intended for high-end signal processing and I/O applications, MORPH features Xilinx Virtex-II Pro® devices.

MORPH products are available in four different varieties. The MORPH VH, and VL offer a single-slot 6U-160 VME64x, the MORPH PH is a single-slot 64-bit universal PCI, and the MORPH PMC is a PCI Bus Mezzanine Card (PMC) design.

MORPH V2P Family

Reconfigurable Signal Processors

FEATURES	MORPH VH	MORPH VL	MORPH PH	MORPH PMC
Form Factor	VME64x	VME64x	64-bit PCI	PMC
Xilinx Virtex-II Pro® XC2VP50	4	2	2	1
Xilinx Virtex-II Pro® XC2VP30		1		
Xilinx Virtex-II Pro® XC2VP20			1	
# of PMC Slots	1	2	2	
P0, P1, P2	√	√		
10/100 Ethernet	√	√		
# of RS-232 ports	8	6	6	2
Off Board MGTS	2	1	0	2
10MHz Reference	√	√	√	
1PPS Input	√	√	√	
PMC MGTs	4	8	8	4
Raceway Support	√	√		
DDR SDRAM	1024 MB	640 MB	512 MB	256 MB
ZBT SRAM	16 MB	8 MB	12 MB	4 MB
Temp Monitoring Circuitry	√	√	√	√
Boot Device	Compact Flash	Compact Flash	PROM	PROM
JTAG	√	√	√	√

Ordering Information

Part Number: MORPH-V2P
 Point of Contact: sales@beecube.com
 510-252-1136

Applications

- **Digital Receiver**
 - Digital Down Converter
 - Re-Sampling
 - CIC / FIR Filters
 - AM, FM, PM Demodulation
- **Frequency Domain Analysis**
 - Fourier Analysis
 - Polyphase Filters
 - Cosine Modulated Filters
- **Linear Combiners**
- **Pulse Characterization / De-interleaving**
- **Hardware acceleration of software applications**

MORPH VH

Reconfigurable Signal Processor



Product Description

The MORPH VH is a board-level product based on reconfigurable logic. Intended for high-end signal processing and I/O applications, this VME64x design features four Xilinx Virtex-II Pro[®] XC2VP50 FPGA devices clocked up to 350 MHz. This FPGA array is interconnected via multi-gigabit serial transceivers (MGTs) and has interfaces to one standard PMC slot, a master/slave VME64 interface, a dual RACE++ interface, and a P0 interface which handles high-speed LVDS and MGT signaling.

Each XC2VP50 features a massive programmable logic array, including over 50,000 flip-flops and their associated combinational logic. Additional embedded functions include two PowerPC[®] 405 cores, 232 18X18 multipliers, 4.2 Mb of Block RAM, 16 MGTs, and sophisticated digital clock management. All four XC2VP50 give MORPH the ability to accommodate board-level designs up to the 5 million gate range. Each FPGA has access to dedicated memory resources which include 256 MB of 133 MHz DDR SDRAM and 4 MB of 166 MHz ZBT SRAM.

A commercial Compact Flash (CF) module is used for non-volatile storage of FPGA configuration data and other software. With a 512 MB CF module, up to 45 configurations may be stored. An automated reconfiguration manager (Xilinx System ACE[®]) supports full reconfiguration of all four FPGAs in under 5 seconds.

The PMC site is a standard 64-bit four-connector site designed to enhance MORPH's reconfigurable capabilities with a wide variety of COTS functions such as A/Ds, high-speed I/O, and auxiliary processors/RAM. It is both 3.3 and 5 volt compliant. Front-panel PMC access allows the use of PCMCIA adapters, if desired.

Features

-4 Xilinx Virtex II Pro[®] XC2VP50 devices each with:

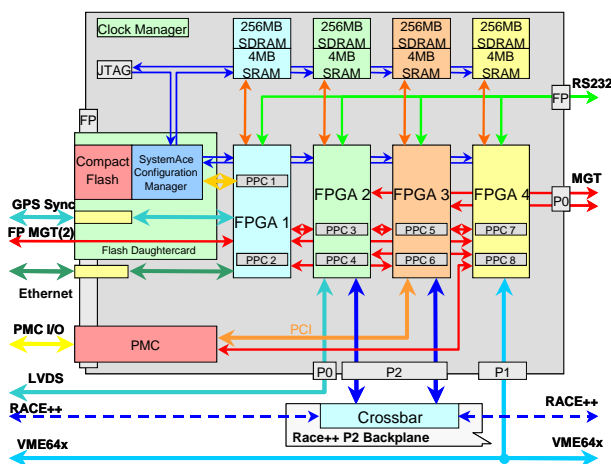
- Implementation for up to 5.0 Mgate designs
- 2 PowerPC[®] 405 Processors with speeds up to 350 MHz
 - 232 18 X 18 Multipliers
 - RAM
 - 4 Mb (internal)
- 256 MB 133 MHz DDR SDRAM
- 4 MB 166 MHz ZBT SRAM

- FPGA Configuration Management

- Compact Flash (Type I or Type II)
- 512 MB CF supports up to 45 configurations
- Reconfiguration in < 5 seconds

- I/O

- PMC: Single 64-bit / 66/33 MHz
- P1: Master/Slave VME64x Interface
- P2: Dual Race++ Signal I/O (532 MBs)
 - P0: LVDS (up to 622 Mbs)
 - Multi-Gigabit Serial (3.125 Gbs)
- 8 RS232 Serial Interfaces
- 10 MHz Reference Clock
- 1 PPS Input
- 2 Off-Board MGTs
- PLL-Based Clock Management
- On Board Temperature Monitoring Circuitry
- Single-Slot 6U-160 VME64x



MORPH VH Block Diagram

Applications

- Digital Receiver
 - Digital Down Converter
 - Re-Sampling
 - CIC / FIR Filters
- AM, FM, PM Demodulation
- Frequency Domain Analysis
 - Fourier Analysis
 - Polyphase Filters
 - Cosine Modulated Filters
- Linear Combiners
- Pulse Characterization / De-interleaving
- Hardware acceleration of software applications

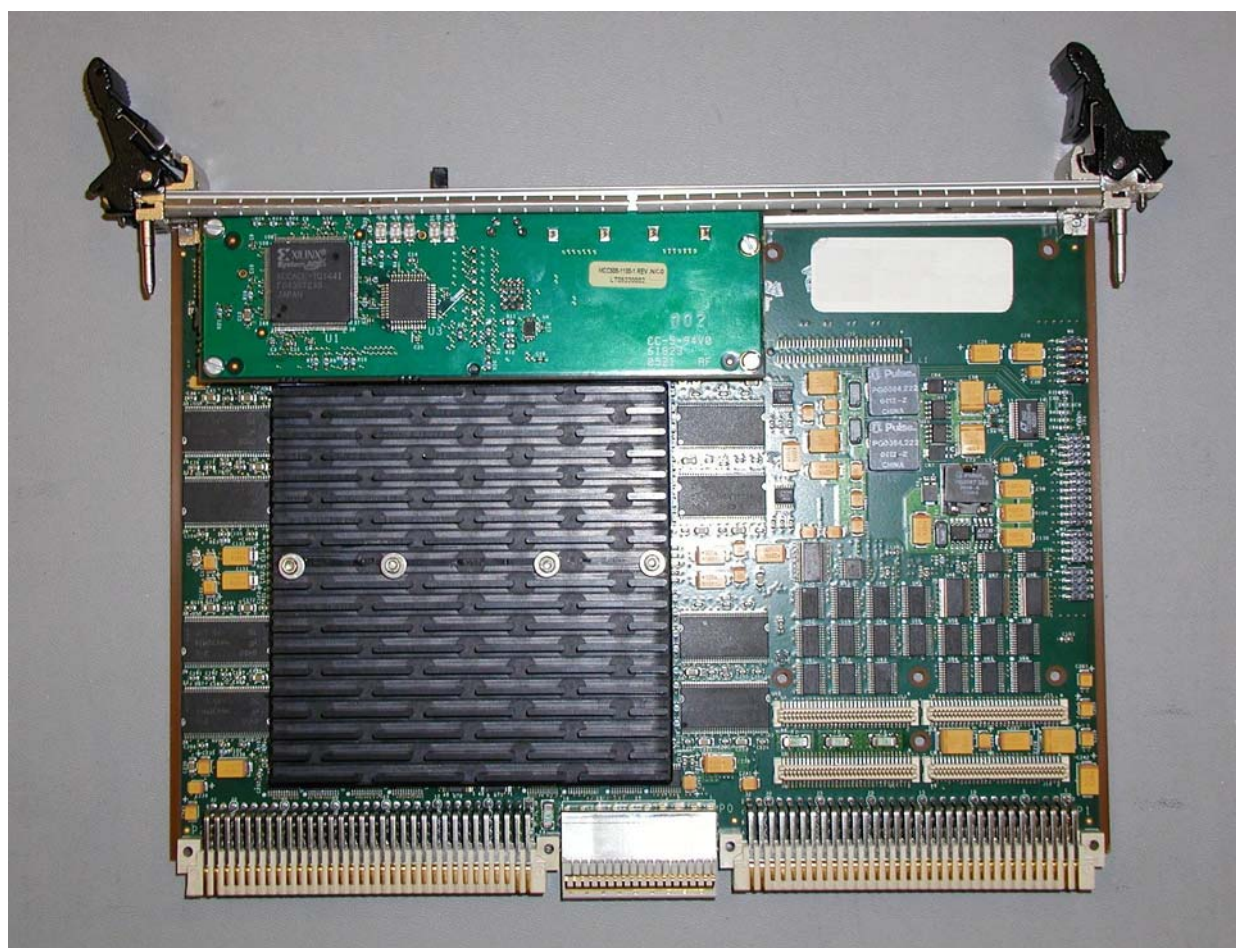
MORPH VH Reconfigurable Signal Processor

Specifications

- **Operating Temperature **0 - 55° C**
- **Altitude **0 - 15,000 feet**
- * Weight **1.5 lbs** (no PMC installed)
- * Input Power **3.3 / 5 VDC**
12VDC (available for PMC)
- * Power Consumption **34 - 55 Watts**
- Dimensions (WHD) **9.0" x 6.0" x 0.75"**
(* May vary depending on configuration.)
(** Design Goal.)

Ordering Information

Part Number: MORPH-V2P-VH
Point of Contact: sales@BEEcube.com
510-252-1136



MORPH VH

MORPH VL

Reconfigurable Signal Processor



Product Description

The MORPH VL is a board-level product based on reconfigurable logic. Intended for high-end signal processing and I/O applications, this VME64x design features two Xilinx Virtex-II Pro[®] XC2VP50 and one XC2VP30 FPGA devices clocked up to 350 MHz. This FPGA array is interconnected via multi-gigabit serial transceivers (MGTS) and has interfaces to two standard PMC slots, a master/slave VME64 interface, a dual RACE++ interface, and a P0 interface which handles high-speed LVDS and MGT signaling.

Each XC2VP50 features a massive programmable logic array, including over 50,000 flip-flops and their associated combinational logic. Additional embedded functions include two PowerPC[®] 405 cores, 232 18X18 multipliers, 4.2 Mb of Block RAM, 16 MGTs, and sophisticated digital clock management. Two of these devices give MORPH the ability to accommodate board-level designs up to the 5 million gate range. Each FPGA has access to dedicated memory resources which include 256 MB of 133 MHz DDR SDRAM and 4 MB of 166 MHz ZBT SRAM. The footprint of the XC2VP50 allows for the FPGA to be downgraded to a XC2VP30.

The XC2VP30 features two PowerPC[®] 405 cores, 136 18X18 multipliers, 2.4 Mb of RAM and includes 128MB of external 133MHz DDR SDRAM. The footprint for the XC2VP30 allows for the FPGA to be downgraded to a XC2VP20.

A commercial Compact Flash (CF) module is used for non-volatile storage of FPGA configuration data and other software. With a 512 MB CF module, up to 45 configurations may be stored. An automated reconfiguration manager (Xilinx System ACE[®]) supports full reconfiguration of all three FPGAs in under 5 seconds.

The PMC sites are standard 64-bit four-connector sites designed to enhance MORPH's reconfigurable capabilities with a wide variety of COTS functions such as A/Ds, high-speed I/O, and auxiliary processors/RAM. It is both 3.3 and 5 volt compliant. Front-panel PMC access allows the use of PCMCIA adapters, if desired.

Features

-2 Xilinx Virtex II Pro[®] XC2VP50 devices each with

- Implementation for up to 5.0 Mgate designs
- 2 PowerPC[®] 405 Processors with speeds up to 350 MHz
 - 232 18 X 18 Multipliers
 - RAM
 - 4.2 Mb (internal)
- 256 MB 133 MHz DDR SDRAM
- 4 MB 166 MHz ZBT SRAM

1 Xilinx Virtex II Pro[®] XC2VP30 device

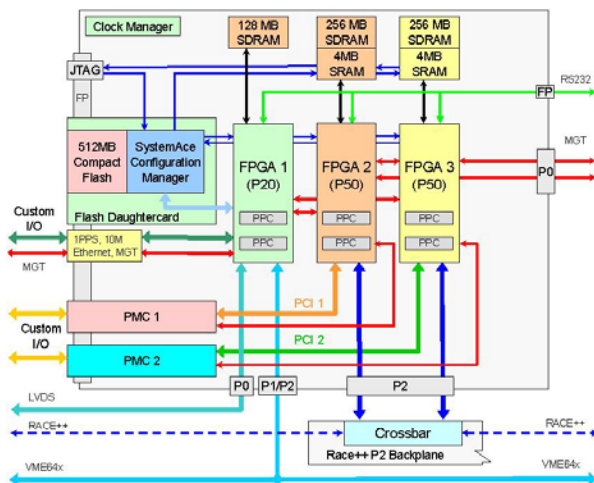
- 2 PowerPC[®] 405 Processors with speeds up to 350 MHz
 - 136 18 X 18 Multipliers
 - RAM
 - 2.4 Mb (internal)
- 128 MB 133 MHz DDR SDRAM
- **FPGA Configuration Management**
 - Compact Flash (Type I or Type II)
 - 512 MB CF supports up to 45 configurations
 - Reconfiguration in < 5 seconds

- I/O

- PMC: Dual 64-bit / 66/33 MHz
 - 1 Off-Board MGT
- P1: Master/Slave VME64x Interface
- P2: Dual Race++ Signal I/O (532 MBs)
 - P0: LVDS (up to 622 Mbs)
 - 6 RS232 Serial Interfaces
 - 10 MHz Reference Clock
 - 1 PPS Input

-PLL-Based Clock Management

- On-Board Temperature Monitoring Circuitry
- Single-Slot 6U-160 VME64x



MORPH VL Block Diagram

Applications

- Digital Receiver

- Digital Down Converter
- Re-Sampling
- CIC / FIR Filters
- AM, FM, PM Demodulation

- Frequency Domain Analysis

- Fourier Analysis
- Polyphase Filters
- Cosine Modulated Filters

-Linear Combiners

-Pulse Characterization / De-interleaving

- Hardware acceleration of software applications

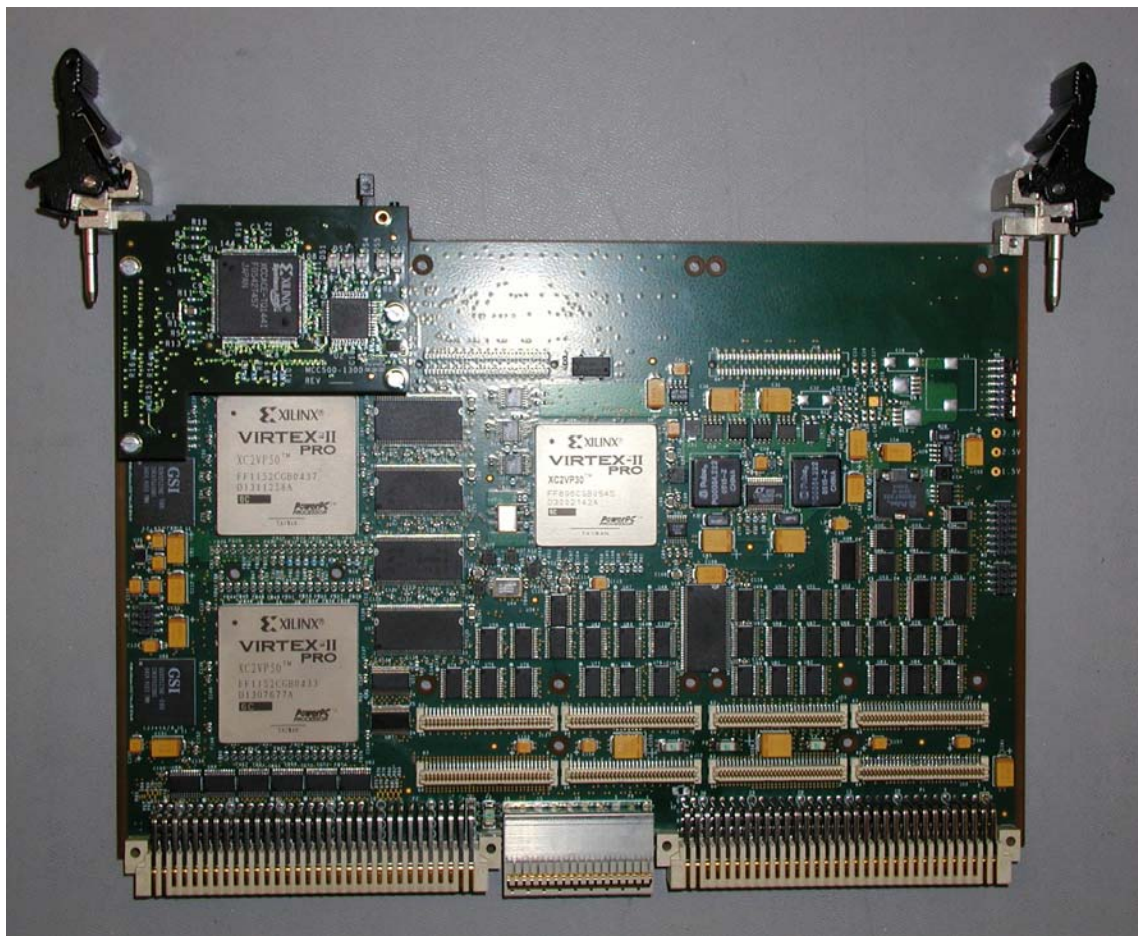
MORPH VL Reconfigurable Signal Processor

Specifications

- **Operating Temperature **0 - 55° C**
- **Altitude **0 - 15,000 feet**
- * Weight **1.34 lbs** (no PMC installed)
- * Input Power **3.3 / 5 VDC**
12VDC (available for PMC)
- * Power Consumption **27 - 46 Watts**
- Dimensions (WHD) **9.0" x 6.0" x 0.75"**
(* May vary depending on configuration.)
(** Design Goal.)

Ordering Information

Part Number: MORPH-V2P-VL
Point of Contact: sales@BEEcube.com
510-252-1136



MORPH VL



MORPH PH

Reconfigurable Signal Processor

Product Description

The MORPH PH is a board-level product based on reconfigurable logic. Intended for high-end signal processing and I/O applications, this PCI design features two Xilinx Virtex-II Pro[®] XC2VP50 and one XC2VP20 FPGA devices clocked up to 350 MHz. This FPGA array is interconnected via multi-gigabit serial transceivers (MGTs) and has interfaces to two standard PMC slots and a 64-bit, 66MHz universal PCI standard edge connector.

Each XC2VP50 features a massive programmable logic array, including over 50,000 flip-flops and their associated combinational logic. Additional embedded functions include two PowerPC[®] 405 cores, 232 18X18 multipliers, 4.2 Mb of Block RAM, 16 MGTs, and sophisticated digital clock management. Two of these devices give MORPH the ability to accommodate board-level designs up to 5 million gate range. Each FPGA has access to dedicated memory resources which include 256 MB of 133 MHz DDR SDRAM and 4 MB of 166 MHz ZBT SRAM. The footprint of the XC2VP50 allows for the FPGA to be downgraded to a XC2VP30.

The XC2VP20 features two PowerPC[®] 405 cores, 88 18X18 multipliers, 1.6 Mb of RAM and includes 4MB of 166MHz ZBT SRAM. The footprint for the XC2VP20 allows for the FPGA to be upgraded to a XC2VP30.

The PMC sites are standard 64-bit four-connector sites designed to enhance MORPH's reconfigurable capabilities with a wide variety of COTS functions such as A/Ds, high-speed I/O, and auxiliary processors/RAM. It is both 3.3 and 5 volt compliant. Front-panel PMC access allows the use of PCMCIA adapters, if desired.

Features

-2 Xilinx Virtex II Pro[®] XC2VP50 devices each with

- Implementation for up to 5.0 Mgate designs
- 2 PowerPC[®] 405 Processors with speeds up to 350 MHz
 - 232 18 X 18 Multipliers
 - RAM
 - 4.2 Mb (internal)
 - 256 MB 133 MHz DDR SDRAM
 - 4 MB 166 MHz ZBT SRAM

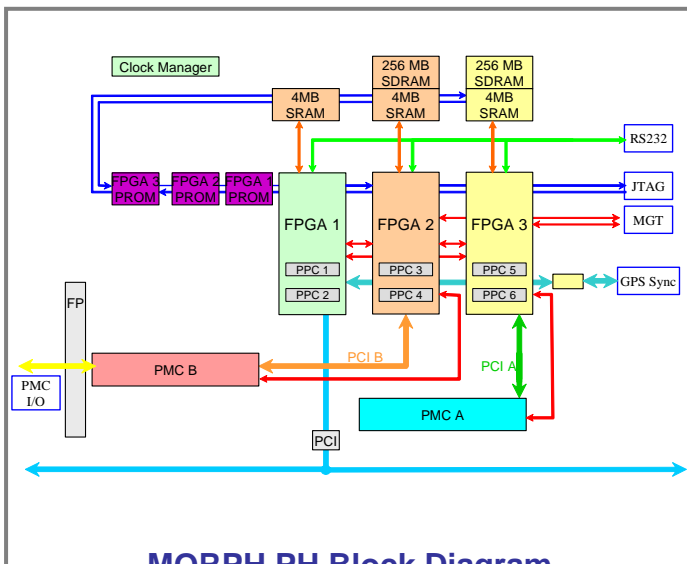
1 Xilinx Virtex II Pro[®] XC2VP20 device

- 2 266 MHz PowerPC[®] 405 Processors
 - 88 18 X 18 Multipliers
 - RAM
 - 1.6 Mb (internal)
 - 4 MB 166 MHz ZBT SRAM

- I/O

- PMC: Dual 64-bit / 66/33 MHz
- 6 RS232 Serial Interfaces
- 10 MHz Reference Clock
- 1 PPS Input

- PLL-Based Clock Management
- On-Board Temperature Monitoring Circuitry
- Single-Slot 64-bit universal PCI



MORPH PH Block Diagram

Applications

- Digital Receiver
 - Digital Down Converter
 - Re-Sampling
 - CIC / FIR Filters
 - AM, FM, PM Demodulation
- Frequency Domain Analysis
 - Fourier Analysis
 - Polyphase Filters
 - Cosine Modulated Filters
- Linear Combiners
- Pulse Characterization / De-interleaving
- Hardware acceleration of software applications

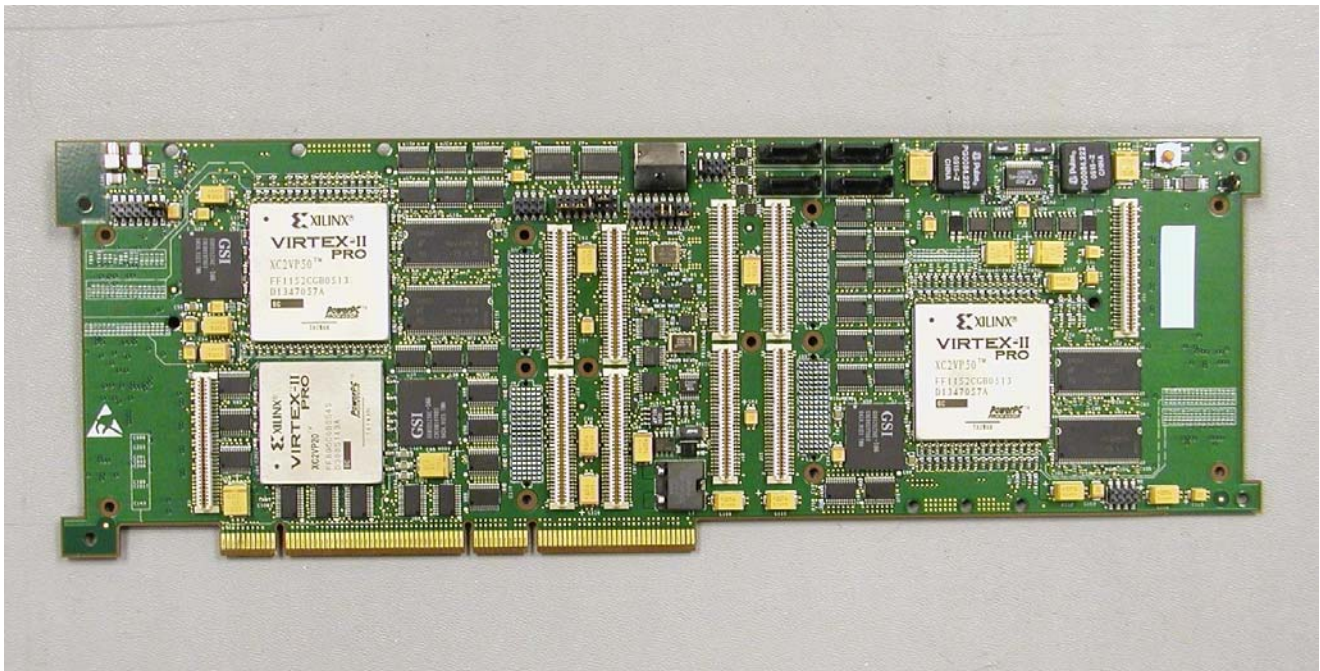
MORPH PH Reconfigurable Signal Processor

Specifications

- **Operating Temperature **0 - 55° C**
- **Altitude **0 - 15,000 feet**
- * Weight **0.6 lbs** (no PMC installed)
- * Input Power **3.3 / 5 VDC**
12VDC (available for PMC)
- * Power Consumption **27 - 46 Watts**
- Dimensions (WD) **12.25" x 4.18"**
(* May vary depending on configuration.)
(** Design Goal.)

Ordering Information

Part Number: MORPH-V2P-PH
Point of Contact: sales@BEEcube.com
510-252-1136



MORPH PH



MORPH PMC

Reconfigurable Mezzanine Card

Product Description

MORPH is a board-level product based on reconfigurable logic. Intended for high-end signal processing and I/O applications, this PCI Bus Mezzanine Card (PMC) design features one Xilinx Virtex-II Pro[®] XC2VP50 FPGA device clocked up to 350 MHz.

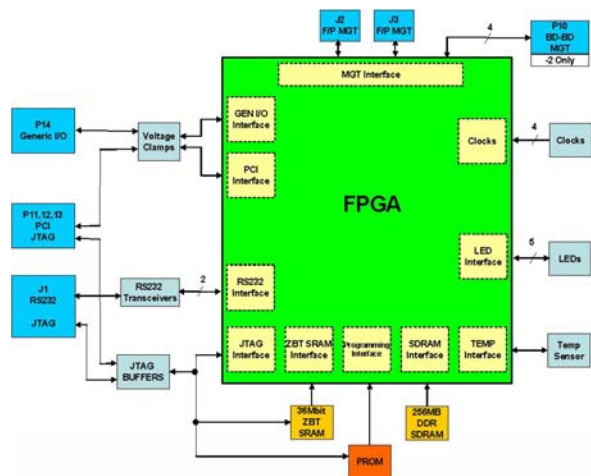
The XC2VP50 features a massive programmable logic array, including approximately 50,000 flip-flops and their associated combinational logic. Additional embedded functions include two PowerPC[®] 405 cores, 232 18X18 multipliers, 4.2 Mb of RAM, 6 high speed serial (MGT) interfaces, and a sophisticated digital clock management system. This device gives the MORPH PMC the ability to accommodate board-level designs up to the 5 million gate range. The FPGA has access to dedicated memory resources which include 256 MB of 266 MHz DDR SDRAM and 4 Mb of 166 MHz ZBT SRAM.

The MORPH PMC is designed according to the P1386.1 specification. It uses the four standard 64-bit connectors for the PCI bus and general I/O that are both 3.3 and 5 volt compliant. The general I/O connector (P14) is available for user defined applications. A fifth connector (P10) is used for four full duplex MGT interfaces between the PMC and host card. Each MGT interface can support data rates up to 3.125 Gb/s in each direction simultaneously.

There are also two full duplex MGT interfaces on the front of the PMC card that are available through standard Serial ATA connectors. A high density 25-pin connector on the front provides access to JTAG signals for test and programming and two RS232 interfaces.

Features

- **1 Xilinx Virtex II Pro[®] XC2VP50 device**
 - Implements up to 5 Mgate designs
 - 232 18 X 18 Multipliers
 - RAM
 - 4 Mb (internal)
 - 256 MB 266 MHz DDR SDRAM
 - 4 MB 166 MHz ZBT SRAM
- **FPGA Configuration Management**
 - Reconfiguration in < 5 seconds
- **I/O**
 - 2 high speed serial interfaces via Serial ATA connectors
 - 64-bits of user defined I/O through P14
 - 4 board to board MGTs via optional P10 connector
 - 2 RS232 serial interfaces
 - JTAG accessible through front panel connector and P11/P12
- **Designed to meet the P1386.1 and IEEE 1386.1 specifications.**
- **External Clock Management Circuitry**
- **Voltage Monitoring LEDs**
- **User Defined LEDs**
- **On-Board Temperature Monitoring Circuitry**



MORPH PMC Block Diagram

Applications

- **Digital Receiver**
 - Digital Down Converter
 - Re-Sampling
 - CIC / FIR Filters
 - AM, FM, PM Demodulation
- **Frequency Domain Analysis**
 - Fourier Analysis
 - Polyphase Filters
 - Cosine Modulated Filters
- **Linear Combiners**
- **PCI RACE interface adapter**
- **Pulse Characterization / De-interleaving**
- **Hardware acceleration of software applications**

MORPH PMC Reconfigurable Mezzanine Card

Specifications

****Operating Temperature** 0 - 55° C
****Altitude** 0 - 15,000 feet
Weight 0.25 lbs
Input Power 5 VDC
*** Power Consumption** 4 - 15 Watts
Dimensions (WHD) 2.91" x 0.5" x 5.86"
(May vary depending on configuration.)*
*(** Design Goal.)*

Ordering Information

Part Number: MORPH-V2P-PMC
Point of Contact: sales@BEEcube.com
510-252-1136



MORPH PMC

www.beecube.com