BEEcube
A National Instruments Company

nanoBEE™

Data Sheet

Figure 1 nanoBEE 4x4

4600 Patrick Henry Drive • Santa Clara, CA 95054 • www.beecube.com

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1. Product Overview

The nanoBEE provides a high-performance, portable and scalable software defined radio (SDR) platform for multi-channel wireless prototyping and MIMO systems in the field testing. The hardware is optimized for worldwide LTE bands supporting both time division duplex (TDD) and frequency division duplex (FDD) operation modes. The nanoBEE is available in two configurations, either remote radio head (RRH) or user equipment (UE), both of which are widely used in infrastructure deployments and fiber to the antenna (FTTA) architectures.
The clocking scheme, based on IEEE 1588v2 protocol, allows multiple antenna nanoBEEs to be dispersed an over multi-kilometer radius while maintaining sub-nano second synchronization and phase coherence, enabling the system to be used for distributed base stations.

2. Details

- Four wideband RF channels:
  - Up to 56 MHz bandwidth per channel
  - RF range covers 70 MHz to 6 GHz
  - 23 dBm output power (2.3~2.7 GHz, 3.3~3.8 GHz and 4.9~5.9 GHz)
  - -94 dBm receiver sensitivity level
- One Xilinx FPGA with two ARM® cores and 2020 DSP slices
- Optimized for LTE cellular RF bands worldwide
- Flexible 2x2 or 4x4 MIMO SDR architectures
- Configurable distributed base stations: RRH and UE categories
- High-accuracy clock synchronization:
  - IEEE 1588v2 based synchronization with sub-ns accuracy via fiber
  - Ultra-low jitter clock source based on IEEE 1588v2 (3ps RMS jitter)
- SDR software compatibility:
  - HDL
  - MATLAB/Simulink
  - C/C++/Python
- Peripherals:
  - 1 GB DDR3 and 4 GB Flash Memory
  - 4x SFP+
  - 1x QSFP
  - 1x HDMI IN and OUT
  - 1x USB v 2.0 (Host)
  - 1x RJ-45 (1G Ethernet)
- Portable form factor

3. APPLICATIONS

- Multi-channel wireless system prototyping:
  - Cellular
  - WiFi
  - L-/S-band SATCOM
- MIMO communications testbeds
- MIMO RADAR systems
- Cognitive radio networks
- White space radios

4. Functional Block Diagram

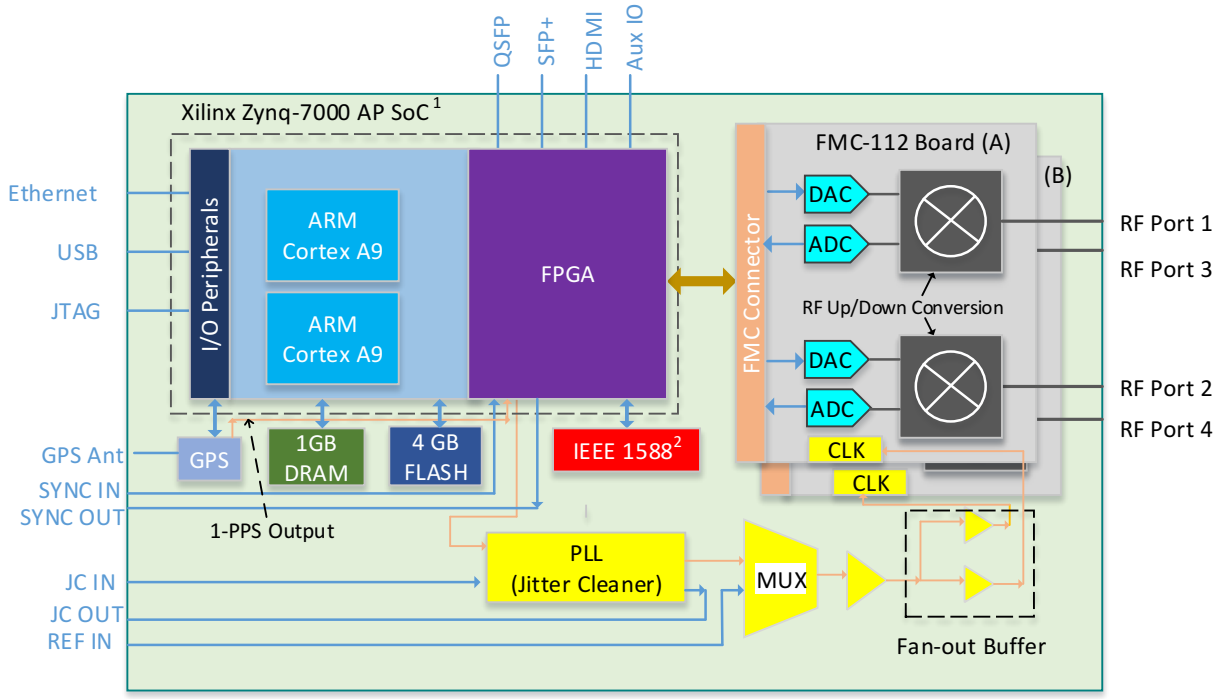

Figure 2 MegaBEE Functional Block Diagram

[1] http://www.xilinx.com/support/documentation/data_sheets/ds190-Zynq-7000-Overview.pdf

[2] The IEEE 1588v2 (Precision Time Protocol, PTP) is implemented on nanoBEE platform using White Rabbit (WR), which is a protocol developed to synchronize nodes in a packet-based network with sub-ns accuracy. The WR is an extension of the PTP (IEEE1588-2008) with automatic precise measurement of the link delay and clock synchronization over the physical layer. http://www.ieee802.org/802_tutorials/2013-07/WR_Tutorial_IEEE.pdf .

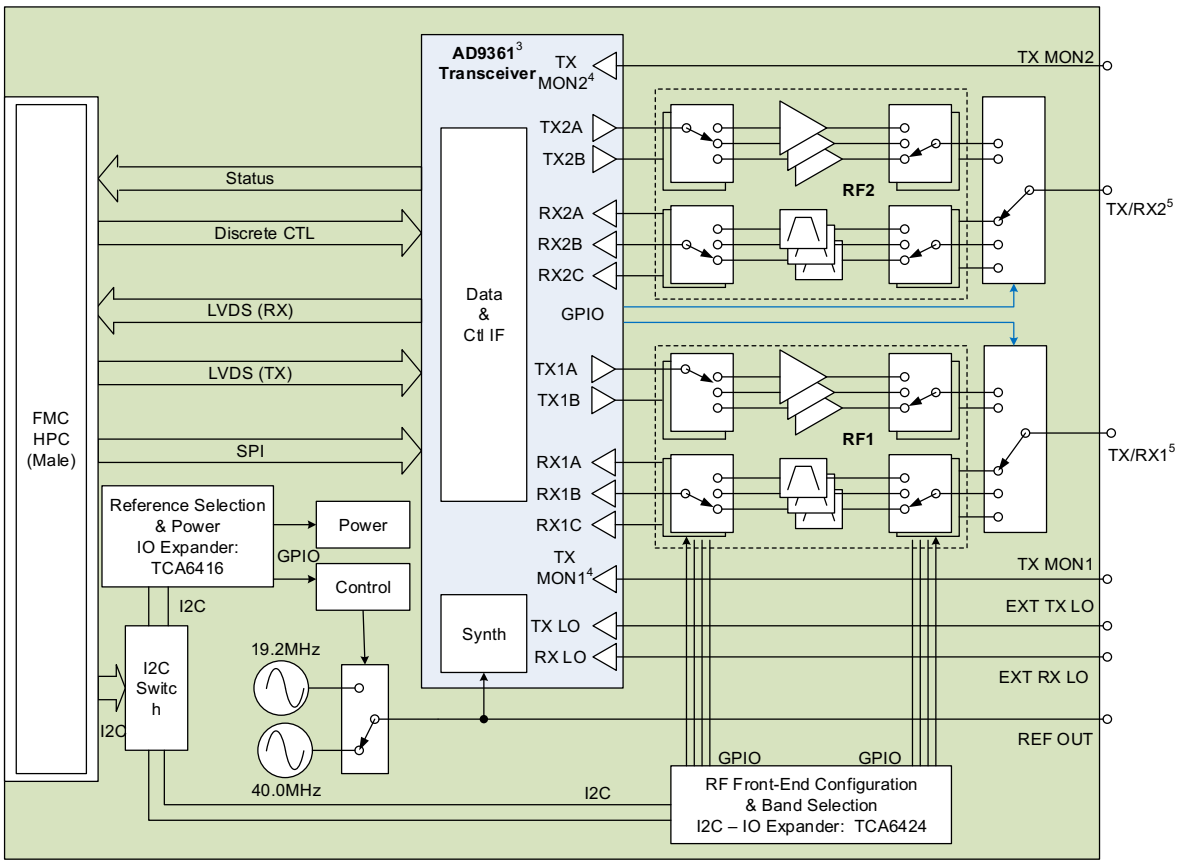

Figure 3 Functional Block Diagram of FMC-112 Board

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[3] http://www.analog.com/media/en/technical-documentation/data-sheets/AD9361.pdf

[4] AD9361 transceiver provides a TX monitor block for each channel (TX MON1/TX MON2). This block monitors the transmitter output and routes it back through an unused RX channel to the baseband for signal monitoring. The TX monitor blocks are available only in TDD mode operation while the RX is idle.

[5] The AD9361 transceiver supports full FDD mode where the TX PLL and the RX PLL can be activated simultaneously. Various combinations of RF switches and band pass filters are selected to switch RF paths between TDD and FDD operation modes. In the FDD TX operation, TX1A/TX2A and TX1B/TX2B DACs are employed for two groups of bands respectively: band 1, 3, 7, WB; U-NII, ISM, 39, 42. In the FDD RX operation mode, RX1B/RX2B ADCs are selected for band 1, 3, 7 and WB, while RX1C/RX2C ADCs are chosen for LTE 38~43, ISM 2.4 GHz and U-NII bands. Please refer to frequency bands for UE and RRH in Table 1 and 2 respectively

5. Frequency Bands Covered

FMC-112 UE[6]				
Band	**TDD/FDD**	**TX Frequency**	**RX Frequency**	**TX Saturation Power (dBm)[7]**
1	FDD	1920-1980	2110-2170	28.45
3	FDD	1710-1785	1805-1880	28.6
7	FDD	2500-2570	2620-2690	26.1
38	TDD	2570-2620	2570-2620	--
39	TDD	1880-1920	1880-1920	28.75
40	TDD	2300-2400	2300-2400	--
41	TDD	2496-2620	2496-2690	--
42	TDD	3400-3600	3400-3600	28.15
43	TDD	3600-3800	3600-3800	--
U-NII	TDD	5150-5825	5150-5825	20.95
ISM 2.4 GHz	TDD	2400-2500	2400-2500	29.7
WB	TDD	70-4000	70-4000	1.2

Table 1 UE Configuration Frequency Bands

FMC-112 RRH[6]				
Band	**TDD/FDD**	**TX Frequency**	**RX Frequency**	**TX Saturation Power (dBm)[7]**
1	FDD	2110-2170	1920-1980	26.05
3	FDD	1805-1880	1710-1785	28.5
7	FDD	2620-2690	2500-2570	25.35
38	TDD	2570-2620	2570-2620	--
39	TDD	1880-1920	1880-1920	28.85
40	TDD	2300-2400	2300-2400	--
41	TDD	2496-2620	2496-2690	--
42	TDD	3400-3600	3400-3600	28.25
43	TDD	3600-3800	3600-3800	--
U-NII	TDD	5150-5825	5150-5825	20.6
ISM 2.4 GHz	TDD	2400-2500	2400-2500	29.7
WB	TDD	70-4000	70-4000	1.5

Table 2 RRH Configuration Frequency Bands

[6]FMC-112 UE and FMC-112 RRH boards are designed and optimized for UE and RRH operation modes respectively.
[7]The saturation transmit power is measured based on FMC-112 Rev.C boards. Attenuation gains are set to zeros. The power values on 38, 40, 41, 43 bands are unavailable and under testing.

6. Specifications[8]

Parameter	Typical Value[9]	Unit	Note
DC Input	12	V	
Power Consumption (Max)	40	W	Power consumption in quiet/standby states will be provided later
ADC/DAC Sample Rate	61.44	Msps	Max sample rate for FMC-112 boards
ADC/DAC Resolution	12	bits	
Frequency Range	70~6000	MHz	
Bandwidth	0.2~56	MHz	
Frequency Stability	+/- 5	ppm	Frequency stability at normal temperature over 24 hours, 19.2 MHz reference clock
Frequency Stability with IEEE 1588 (short-term)	+/-1	ppb	Frequency stability at normal temperature over 100 seconds
Frequency Stability with IEEE 1588 (long-term)[10]	+/-83	ppb	Frequency stability at normal temperature over 50 hours
Transmitters			
Transmit Power	25.6	dBm	1MHz tone, 50 Ohm load, carrier frequency 2.55 GHz, 3GPP UE power class 3 [11]
OIP3 (Third-Order Output Intermodulation)[12]	41	dBm	See AVAGO MGA-22003 data sheet. IP3 is usually 10dB higher than the 1dB compression point of the nonlinear RF device.
1dB Compression Point[12]	31	dBm	See AVAGO MGA-22003 datasheet.
Modulation Accuracy, EVM			
2.55 GHz	-40	dB	10 dB attenuation, 19.2 MHz reference clock
5.8 GHz	-35	dB	10 dB attenuation, 19.2 MHz reference clock
Carrier Leakage[13]	-50	dBc	0 dB attenuation, carrier frequency 2.4 GHz
Receivers			
Noise Figure, NF[14]	7	dB	Maximum RX gain, carrier frequency 2.55 GHz
IIP3 (Third-Order Input Intermodulation)[13]	−14	dBm	Maximum RX gain, carrier frequency 2.4 GHz
IIP2 (Second-Order Input Intermodulation)[13]	45	dBm	Maximum RX gain, carrier frequency 2.4 GHz
Integrated Phase Noise			
2.55 GHz	1	deg rms	10 dB attenuation, 19.2 MHz reference clock
5.8 GHz	1.8	deg rms	10 dB attenuation, 19.2 MHz reference clock
Isolation between RX RF Channels[13]	>50	dB	Maximum RX gain
Receiver Sensitivity Level	-94	dBm	QPSK modulation, maximum RX gain, carrier frequency 2.55GHz @BER=10^{-2} (uncoded)

Table 3 Specifications of nanoBEE

[8] All specifications may be updated.
[9] Parameters and typical values dependent on test conditions: bands, RX gains, clock frequency and temperature. All values are evaluated at room temperature, unless stated otherwise.
[10] Brückner, M., and R. Wischnewski. "A White Rabbit setup for sub-nsec synchronization, timestamping and time calibration in large scale astroparticle physics experiments." Proceedings of the 33rd ICRC, Rio de Janeiro, paper 1146.
[11] http://www.etsi.org/deliver/etsi_ts/136100_136199/136101/10.03.00_60/ts_136101v100300p.pdf
[12] Estimates from data sheets of Avago's power amplifiers. Actual measurements are under testing and to be announced.
[13] Estimates from data sheets of AD9361 chip. Actual measurements are under testing and to be announced.
[14] Estimates based on cascade analysis using data sheets of RF components in the receive path. Actual measurements are under testing and to be announced.

Port Name	Type	Function
CLK OUT (B)	SMA	Reference clock output from FMC-112 board B
RX-LO (B)	SMA	RX LO frequency for FMC-112 board B
TX-LO (B)	SMA	TX LO frequency for FMC-112 board B
CLK OUT (A)	SMA	Reference clock output from FMC-112 board A
RX-LO (A)	SMA	RX LO frequency for FMC-112 board A
TX-LO (A)	SMA	TX LO frequency for FMC-112 board A
REF CLK IN	SMA	Reference clock input for Group 1 baseboard
JC CLK IN	SMA	Reference clock input to jitter cleaner block
JC CLK OUT	SMA	Reference clock output from jitter cleaner block
SYNC IN	SMA	Synchronization signal input (2.5 Vdc)
SYNC OUT	SMA	Synchronization signal output (2.5 Vdc)
RF 1	SMA	RF port 1
RF 2	SMA	RF port 2
RF 3	SMA	RF port 3
RF 4	SMA	RF port 4
GPS ANT	SMA	GPS antenna port
USB JTAG	Micro Type B Jack	JTAG interference for FPGA in Group 1
MICRO SD	micro SD	Micro SD card for Group 1 baseboard
AUX I/O L	MiniHDMI	I/O interface for auxiliary I/O pins (left side)
AUX I/O R	MiniHDMI	I/O interface for auxiliary I/O pins (right side)
CLK OUT (D)	SMA	Reference clock output from FMC-112 board D
RX-LO (D)	SMA	RX LO frequency for FMC-112 board D
TX-LO (D)	SMA	TX LO frequency for FMC-112 board D
CLK OUT (C)	SMA	Reference clock output from FMC-112 board C
RX-LO (C)	SMA	RX LO frequency for FMC-112 board C
TX-LO (C)	SMA	TX LO frequency for FMC-112 board C
REF CLK IN	SMA	Reference clock input for Group 2 baseboard
JC CLK IN	SMA	Reference clock input to jitter cleaner block
JC CLK OUT	SMA	Reference clock output from jitter cleaner block
SYNC IN	SMA	Synchronization signal input (2.5 Vdc)
SYNC OUT	SMA	Synchronization signal output (2.5 Vdc)
RF 5	SMA	RF port 5
RF 6	SMA	RF port 6
RF 7	SMA	RF port 7
RF 8	SMA	RF port 8
GPS ANT	SMA	GPS antenna port
REF CLK OUT 1	SMA	Reference clock out 1 (fan-out buffer)
REF CLK OUT 2	SMA	Reference clock out 1 (fan-out buffer)
REF CLK OUT 3	SMA	Reference clock out 1 (fan-out buffer)
REF CLK OUT 4	SMA	Reference clock out 1 (fan-out buffer)
USB JTAG	Micro Type B Jack	JTAG interference for FPGA in Group 2
MICRO SD	micro SD	Micro SD card for Group 2 baseboard
AUX I/O L	MiniHDMI	I/O interface for auxiliary I/O pins (left side)
AUX I/O R	MiniHDMI	I/O interface for auxiliary I/O pins (right side)

Table 4 Table of Input and Output Ports (front panel)

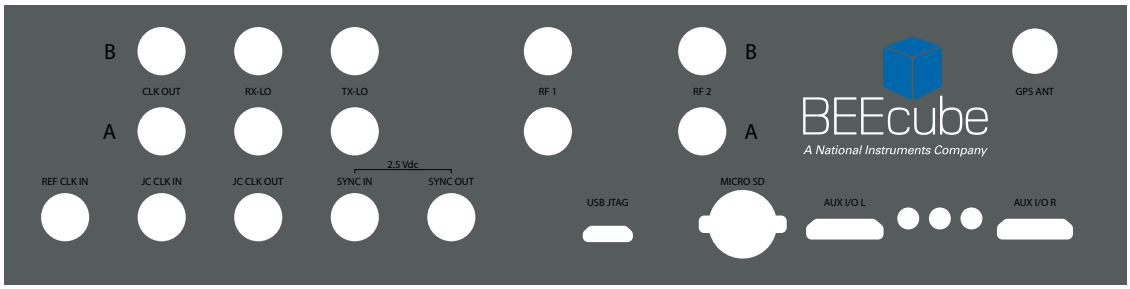

Figure 4 nanoBEE 4x4 Front Panel

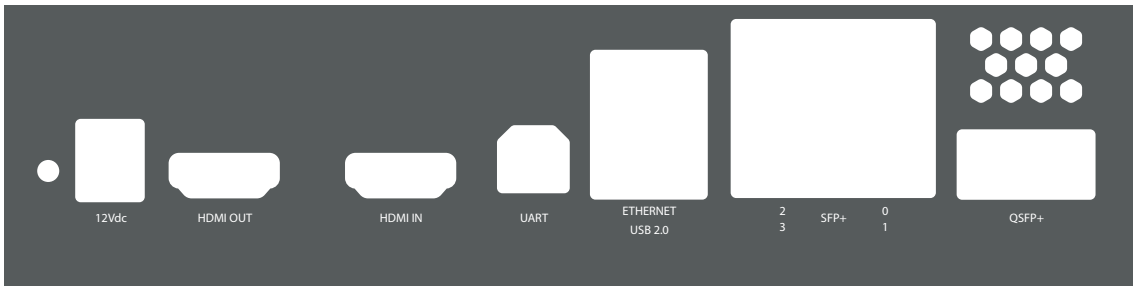

Figure 5 nanoBEE Rear Panel

Port Name	Type	Function
HDMI OUT	HDMI	HDMI output port
HDMI IN	HDMI	HDMI input port
USB 2.0 Device	2.0 Type B Jack	USB 2.0 device port
ETHERNET	Ethernet port	Ethernet connection to each group
USB 2.0 HOST	2.0 Type A Jack	USB 2.0 host port
SFP+ 0	SFP	SFP+ port 0
SFP+ 1	SFP	SFP+ port 1
SFP+ 2	SFP	SFP+ port 2
SFP+ 3	SFP	SFP+ port 3
QSFP+	QSFP	QSFP+ port

Table 5 Table of Input and Output Ports (rear panel)